Abstracts

Binary Peak Power Multiplier and its Application to Linear Accelerator Design

Z.D. Farkas. "Binary Peak Power Multiplier and its Application to Linear Accelerator Design." 1986 Transactions on Microwave Theory and Techniques 34.10 (Oct. 1986 [T-MTT] (Special Issue on New and Future Applications of Microwave Systems)): 1036-1043.

This paper describes a new method of pulse compression, the binary power multiplier (BPM), a device which multiplies RF power in binary steps. It comprises one or more stages, each of which doubles the input power and halves the input pulse length. Practical designs are described and expressions for their compression efficiency are derived. The usefulness of pulse compression for accelerator design is illustrated and compared with the pulse compression system currently in use at the Stanford Linear Accelerator Center.

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